What is claimed is:

1. A method of forming solder bumps on a microelectronic device having a semiconductor substrate and a contact pad on said semiconductor substrate, wherein said contact pad has an exposed surface portion, said method comprising the steps of:

providing said semiconductor substrate, the surface of said substrate having been provided with a least one contact pad having a surface;

depositing a layer of passivation over the surface of said substrate including said exposed surface of said contact pad;

patterning and etching said layer of passivation, partially exposing said surface of said contact pad;

depositing a conductive layer over the surface of said layer of passivation, including said partially exposed surface of said contact pad;

patterning and etching said conductive layer, removing said conductive layer from above said layer of passivation, partially exposing the surface of said layer of passivation, leaving said conductive layer in place above and extending from above said contact pad by a measurable amount, creating a conductive layer overlying said contact pad;

depositing a layer of elastomer over said partially exposed surface of said layer of passivation, including the surface of said conductive layer overlying said contact pad;

patterning and etching said layer of elastomer, creating an opening in said layer of elastomer that aligns with and exposes the surface of said conductive layer overlying said contact pad;

depositing a layer of solder or solder compound over the exposed surface of said conductive layer; and

performing a process of reflow, simultaneously curing said deposited layer of solder or solder compound and said patterned and etched layer of elastomer.

2. The method of claim 1 wherein said layer of passivation comprises PE Si_3N_4 deposited to a thickness between about 200 and 800 Angstrom.

3. The method of claim 1 wherein said layer of passivation is selected from the group comprising the materials SiO_2, a photosensitive polyimide, phosphorous doped silicon dioxide and titanium nitride deposited to a thickness between about 200 and 800 Angstrom.

4. The method of claim 1 wherein said conductive layer comprises a layer of Under Bump Metallurgy comprises a layer of chromium followed by a layer of copper followed by a layer of gold.

5. The method of claim 4 wherein said layer of Under Bump Metallurgy comprises a layer of chromium followed by a layer of copper followed by a layer of gold.

6. The method of claim 4 wherein said layer of Under Bump Metallurgy comprises a plurality of sub-layers of different metallic composition.

7. The method of claim 1 wherein said elastomer comprises a polymer.

8. The method of claim 1 wherein said passivation layer deposited over the surface of said semiconductor surface comprises a plurality of passivation layers.

9. The method of claim 8 wherein at least one of said plurality of passivation layers is selected from a group comprising PE Si_3N_4, SiO_2, a photosensitive polyimide, phosphorous doped silicon dioxide and titanium nitride.

10. The method of claim 1 wherein said contact pad on said semiconductor surface is electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

11. The method if claim 1 wherein said depositing a layer of elastomer is applying a layer of liquid elastomer by spinning elastomer over the surface of the passivation layer including the surface of the etched layer of conductive material.

12. The method if claim 1 wherein said depositing a layer of elastomer is applying a dry film of elastomer laminated over the surface of the passivation layer, including the surface of the etched layer of conductive material.

13. The method if claim 1 wherein said depositing a layer of elastomer is applying a patterned layer of elastomer by laminating said elastomer as a tape film that is aligned with the contact pad, said lamination to occur over the surface of the passivation layer, including the surface of the etched layer of conductive material.

14. The method if claim 1 wherein said depositing a layer of elastomer is applying a patterned layer of elastomer by laminating said elastomer as an elastomer film in which via openings have been formed over the surface of the passivation layer, including the surface of the etched layer of UBM.

15. The method of claim 1 wherein said contact pad on said semiconductor substrate is further expanded to include a contact pad that is formed on a surface that is selected from a group of surfaces comprising printed circuit boards, flex circuits or a metallized or glass substrate or semiconductor device mounting support.

16. The method of claim 1 with the additional step of performing an in-situ sputter clean of said conductive layer overlying said contact pad, said additional step to be performed after said step of patterning and etching said layer of elastomer.

17. The method of claim 1 with the additional step of depositing a seed layer over the surface of said layer of conductive material, said additional step to be performed after said layer of conductive material has been deposited.

18. The method of claim 1 with the additional step of depositing a solder flux or paste over said deposited layer of solder or solder compound, said additional step to be performed after said layer of solder or solder compound has been deposited.

19. The method of claim 1 wherein said patterning and etching said conductive layer leaving said conductive layer in place

above and extending from above said contact pad by a measurable amount is further expanded to simultaneously create conductive interconnect lines on the surface of said layer of passivation, said conductive interconnect lines to make contact with at least one contact pad on said semiconductor substrate by creating openings in said layer of passivation that align with at least one contact pad on said semiconductor substrate.

20. A method of forming solder bumps on a microelectronic device having a semiconductor substrate and a contact pad on said semiconductor substrate, wherein said contact pad has an exposed surface portion, said method comprising the steps of:

providing said semiconductor substrate, the surface of said substrate having been provided with a least one contact pad having a surface;

depositing one or more layers of passivation over the surface of said substrate including said exposed surface of said contact pad;

patterning and etching said on or more layers of passivation, partially exposing said surface of said contact pad;

depositing a conductive layer comprising Under Bump Metallurgy comprising one or more of sub-layers of different metallic composition over the surface of said one or more layers

of passivation, including said partially exposed surface of said contact pad;

patterning and etching said conductive layer, removing said conductive layer from above said layer of passivation, partially exposing the surface of said layer of passivation, leaving said conductive layer in place above and extending from above said contact pad by a measurable amount, creating a conductive layer overlying said contact pad;

depositing a layer of elastomer or any other suitable polymer over said partially exposed surface of said one or more layers of passivation including the surface of said conductive layer overlying said contact pad by methods of spinning or dry film deposition or elastomer tape film deposition or by patterned layer of elastomer deposition;

patterning and etching said layer of elastomer, creating an opening in said layer of elastomer that aligns with and exposes the surface of said conductive layer overlying said contact pad;

depositing a layer of solder or solder compound over the exposed surface of said conductive layer; and

performing a process of reflow, simultaneously curing said deposited layer of solder or solder compound and said patterned and etched layer of elastomer.

21. The method of claim 19 with the additional step of performing an in-situ sputter clean of said conductive layer overlying said contact pad, said additional step to be performed after said step of patterning and etching said layer of elastomer.

22. The method of claim 19 with the additional step of depositing a seed layer over the surface of said layer of conductive material, said additional step to be performed after said layer of conductive material has been deposited.

23. The method of claim 19 with the additional step of depositing a solder flux or paste over said deposited layer of solder or solder compound, said additional step to be performed after said layer of solder or solder compound has been deposited.

24. The method of claim 19 wherein said patterning and etching said conductive layer leaving said conductive layer in place above and extending from above said contact pad by a measurable amount is further expanded to simultaneously create conductive interconnect lines on the surface of said layer of passivation, said conductive interconnect lines to make contact with at least one contact pad on said semiconductor substrate by creating openings in said layer of passivation that align with at least one contact pad on said semiconductor substrate.

25. A conductive bump overlying a layer of Under Bump Metallization (UBM) formed in electrical contact with at least one contact pad underlying at least one via defined in at least one layer of passivation deposited over a semiconductor substrate, comprising:

providing said semiconductor substrate including integrated circuitry therein, and at least one layer of passivation having a thickness deposited over the surface of said semiconductor substrate;

providing access to said integrated circuitry for external contact by forming at least one via having a diameter extending through said at least one layer of passivation, partially exposing the surface of said at least one contact pad;

performing an in-situ sputter clean of the partially exposed surface of the at least one contact pad;

forming a substantially conformal layer of UBM metal having a thickness over said at least one layer of passivation with a portion of said layer of UBM metal extending into said at least one via to make electrical contact with said at least one contact pad;

defining a partially exposed surface of said layer of UBM that is aligned with said at least one contact pad by depositing, patterning and etching a layer of etch blocking material over the surface of said semiconductor surface, removing said first layer

of etch blocking material from above surface areas of said layer of UBM that do not belong to the surface of said first partially exposed surface of said layer of UBM;

etching said layer of UBM, removing said etched layer of UBM from the surface of said semiconductor surface where this layer of UBM does not belong to said first partially exposed surface of said layer of UBM, creating a partially exposed layer of UBM, partially exposing the surface of said layer of passivation;

removing said patterned and etched first layer of etch blocking material from the above the surface of said semiconductor surface;

depositing a layer of elastomer or any other suitable polymer over said partially exposed layer of UBM, thereby including the surface of said partially exposed layer of passivation;

patterning and etching said layer of elastomer or any other suitable polymer, creating at least one opening in said layer of elastomer or any other suitable polymer that aligns with and exposes the surface of said partially exposed surface of said layer of UBM;

filling said at least one opening created in said layer of elastomer or any other suitable polymer with a solder compound or its alloy;

applying a flux to the surface of said solder compound or

its alloys; and

reflowing the surface of said layer of solder or its alloys, forming the solder bump, curing said elastomer or any other suitable polymer.

26. The conductive bump of claim 25 wherein said layer of etch blocking material comprises photoresist.

27. The conductive bump of claim 25 with the additional step of plating a conductive material over the surface of said partially exposed surface of said layer of UBM, said additional step to be performed prior to said step of filling said opening created in said layer of second etch blocking material with a solder compound or its alloy.

28. The conductive bump of claim of claim 27 wherein said conductive material comprises a metal.

29. The conductive bump of claim 25 wherein said at least one layer of passivation comprises PE Si_3N_4 deposited to a thickness between about 200 and 800 Angstrom.

30. The conductive bump of claim 25 wherein at least one of said at least on layers of passivation is selected from the group

comprising the materials PE Si_3N_4, SiO_2, a photosensitive polyimide, phosphorous doped silicon dioxide and titanium nitride deposited to a thickness between about 200 and 800 Angstrom.

31. The conductive bump of claim 25 wherein said layer of Under Bump Metallurgy comprises a layer of chromium followed by a layer of copper followed by a layer of gold.

32. The conductive bump of claim 25 wherein said layer of Under Bump Metallurgy comprises a plurality of sub-layers of different metallic composition wherein at least one of said plurality of sub-layers comprises titanium and at least one of said plurality of sub-layers comprises copper.

33. The conductive bump of claim 25 wherein said contact pad on said semiconductor surface is electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

34. The conductive bump of claim 25 wherein said etching said layer of partially exposed layer of UBM to create said first partially exposed surface of said layer of UBM comprises methods of sputter etching or wet etching.

35. The conductive bump of claim 25 wherein said surface of said semiconductor substrate is expanded to surfaces that are selected from a group of surfaces comprising semiconductor substrates, printed circuit boards, flex circuits or a metallized or glass substrate or semiconductor device mounting support.

36. The method of claim 25 with the additional step of performing an in-situ sputter clean of said conductive layer overlying said contact pad, said additional step to be performed after said step of patterning and etching said layer of elastomer.

37. The method of claim 25 with the additional step of depositing a seed layer over the surface of said substantially conformal layer of UBM, said additional step to be performed after said layer of substantially conformal layer of UBM been deposited.

38. The method of claim 25 said wherein etching said layer of UBM creating a partially exposed layer of UBM is further expanded to simultaneously create conductive interconnect lines on the surface of said on or more layers of passivation, said conductive interconnect lines to make contact with at least one contact pad on said semiconductor substrate by creating openings in said one or more layers of passivation that align with at least one contact pad on said semiconductor substrate.